Sub Code: **ROLL NO.**

MODEL QUESTION PAPER

COURSE: M.TECH **BRANCH**: VLSI Design

SEMESTER: 1nd **SUBJECT**: Low Power VLSI Design

Duration: 3:00 hrs **Max marks: 100**

Note: - Attempt all questions: All Questions carry equal marks

Q 1.Attempt any four parts of the following (5x4=20)

(a) Explain the limitation in low power circuit design.
(b) State the advantages and disadvantages of BICMOS Technology.
(c) What is punch-through is MOSFET?
(d) Discuss the advantage of SIMOX technique in present low power design scenario.
(e) Explain SOI technique and its advantage.
(f) Discuss the disadvantage of Twin Well BiCOMS integration process.

Q 2.Attempt any four parts of the following (5x4=20)

(a) Explain LOCOS isolation technique. What are its limitations?
(b) We prefer copper metallization over aluminum in low power technology why?
(c)Explain the dynamics characteristics of MOS.
(d) What are the device modeling considerations?
(e) Explain domino logic design modeling.
(f) What are merged BiCMOS digital circuits?

Q 3.Attempt any two parts of the following (10x2=20)

(a) How will you fabricate low cost, medium speed 5V digital BICMOS.
(b) Explain BICMOS isolation techniques.
(c) Explain Gummel-Poon model.

Q4.Attempt any two parts of the following: (10x2=20)

(a) Design the bi CMOS NAND gate.
(b) What are the quality measures for Latches and Flip-Flop?
(c) What is ESD free device? Design ESD free Bi COMS inverter.

Q5.Attempt any two parts of the following: (10x2=20)

(a) Explain clock gating technique.
(b) How will you reduce power dissipation in clocked network? Explain one of the technique.
(c) Discuss the evolution themes of Flop Flop .