Sub Code: VDT-302 **ROLL NO.**

Model Question Paper

COURSE: M.TECH **BRANCH**: VLSI DESIGN

SEMESTER: 1 **SUBJECT**: Digital System Design Using Verilog

Duration: 3:00 hrs **Max marks: 100**

Note: Attempt all questions.

1. **Attempt any four parts of the following question. 5x4 = 20**

   A. What do you understand by Electronic Design Automation? Also, give the importance of HDls.

   B. Realize the following Boolean Expression using CMOS logic:

      (i) OR Gate

      (ii) XOR Gate

   C. Name the different system task used in Verilog. What is the different between $monitor and $display.

   D. Explain Synthesis and simulation process used in cad tools.

   E. Different between front end and back end design tools used for Verilog design. Also explain Instances.

   F. Explain different levels of abstraction for electronic design. Elucidate important design methods for IC design.

2. **Attempt any four parts of the following question. 5x4 = 20**

   A. Explain different white space used in Verilog.

   B. What do you understand by comments used in Verilog .Also explain different comments used in Verilog.

   C. How many types of number specification in Verilog. Explain it.

   D. Explain Integer, Real, and Time register data types used in Verilog.

   E. Explain vectors part select and Variable Vector Part Select used in Verilog.

   F. Explain Stopping and finishing system task in a simulation.

3. **Attempt any two parts of the following question. 10x2 = 20**

   A. Write down the Verilog code for 4-to-1 Multiplexer using Behavioral modelling.

B. Write down the Verilog code for 4-to-1 multiplexer using logic equation or using conditional operator in data flow modelling.

C. Explain blocking and non-blocking assignment used in Verilog.

4. **Attempt any two parts of the following question. 10x2 = 20**

A. Explain user define primitive and different types of user define primitive defined in Verilog.

B. Write a short note on the following.
(i) Casex and casez statement
(ii) Power and Ground
(iii) Parallel connection and full connection

C. What is the difference between continuous assignment and implicit continues assignment? Also, explain three methods to assign a delay.

5. **Attempt any two parts of the following question. 10x2 = 20**

A. Define a finite state machine with the help of proper diagram. Also, give its classification in detail.
B. Describe the procedure/steps of adding and removing task from the queue.
C. Explain gate delay used in Verilog with suitable example. Also a Verilog code for 4-bit counter using behavioral modelling.

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